We claim:

1. A programmable processor comprising:

an instruction path;

a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a register file operable to receive and store data from the data path and communicate the stored data to the data path; and

an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single instruction specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register, the execution unit is operable to:

(i) detect some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and

(ii) cause the write-enabled data fields to be written to a specified memory location.

2. The processor of claim 1 wherein each of the fields of the mask has a width of one bit.

3. The processor of claim 1 wherein each of the fields of the data contained in the register has a width of one bit.

4. The processor of claim 1 wherein the execution unit is operable to cause the write-enabled data fields to be written to the specified memory location by reading an unaltered field

of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location.

5. The processor of claim 1 wherein the mask is contained in a specified register.

6. The processor of claim 1 wherein the memory location is contained in a specified register.

7. The processor of claim 1 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

8. The processor of claim 1 wherein the predetermined value is a logic 1.

9. The processor of claim 1 wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a third and a fourth register each containing a plurality of operands, multiply the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products and provide the plurality of products to partitioned fields of a result register as a second catenated result.

10. A data processing system comprising:

(a) a bus coupling components in the data processing system;

(b) an external memory coupled to the bus;

(c) a programmable microprocessor coupled to the bus and capable of operation

independent of another host processor, the microprocessor comprising:

an instruction path;

a data path;

an external interface operable to receive data from an external source and communicate the received data over the data path;

a register file operable to receive and store data from the data path and communicate the stored data to the data path; and

an execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path, wherein in response to decoding a single instruction specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register, the execution unit is operable to:

(i) detect some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and

(ii) cause the write-enabled data fields to be written to a specified memory location.

11. The system of claim 10 wherein each of the fields of the mask has a width of one bit.

12. The system of claim 10 wherein each of the fields of the data contained in the register has a width of one bit.

13. The system of claim 10 wherein the execution unit is operable to cause the write-enabled data fields to be written to the specified memory location by reading an unaltered field of data

from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location.

14. The system of claim 10 wherein the mask is contained in a specified register.

15. The system of claim 10 wherein the memory location is contained in a specified register.

16. The system of claim 10 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

17. The system of claim 10 wherein the predetermined value is a logic 1.

18. The system of claim 10 wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a third and a fourth register each containing a plurality of operands, multiply the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality of products and provide the plurality of products to partitioned fields of a result register as a second catenated result.